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Platune: A Tuning Framework for System-on-a-Chip Platforms - Givargis, Vahid (2002) (Correct) (8 citations)
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of a finite abstract group"Proc. Edinburgh Math. **Soc**.5, 26-34. Helmut Wielandt (1964)Finite 4 subgroup, 4 subspace, 58 symmetric group, 4 **timing**, 49 Todd-Coxeter algorithm, 7 Todd-Coxeter 7 Todd-Coxeter Schreier-Sims algorithm, 34 **trace** algorithm, 18 trivial group, 4 var statement, 5
www.mathe2.uni-bayreuth.de/axel/papers/./murray:the_schreier_sims_algorithm.ps

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two con icting trends: The transistor count of **SoCs** is exponentially growing -allowing ever above. Thus, it leads to the shorter simulation **time** while it can still give fairly accurate The symbolic program approach is based on both the **trace** driven approach and the control data ow graph
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microprocessorbased board. Such Systems-on-Chip (**SoC**) are heterogeneous, that is, they are embedding said that more effort at the system-level -to cut "**time**-to-market" is urgently needed. We agree and consisting of a symbolic program and a control **trace**. I. INTRODUCTION Today's embedded systems are
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An Adaptive Silicon Synapse - Elisabetta Chicca Giacomo (2003) (Correct)
and present experimental results measured from a **chip** fabricated using a standard 1.5m CMOS technology. the dynamic modulation of synaptic strength by the **timing** of the input stimulation [7]Although there has of Vw d (see lower left inset in graph)Each **trace** is normalized with respect to its maximum EPSP
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the verification problems that large systems on **chip** have. CAKE is formed by a set of equal tiles. Each
. 47 5.2.2 **Time** Criticality Diagram .
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optimal concerning speed, but usually need much **chip** area. Embedded systems often cannot deal with the multiplication in embedded systems stood often for **time**-consuming and place-ineffective tasks, general technology. Therefore, we decided to split the **trace** of related work into two sections: architectures
wwwcs.upb.de/fachbereich/AG/rammig/www/members/berndk/./PS/nasa03-const-mult.pdf

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C/A signal, the DLL precision is approximately of 1 **chip**, and one data symbol is composed of 1023 **chips**, Box 1116, D-82230 Wessling, Germany ABSTRACT The **time**-of-arrival estimation error produced by multipath #8) where "is the **trace** operator, and we have omitted the dependency
mti.xidian.edu.cn/multimedia/2001/supp/icassp2001/MAIN/papers/pap1064.pdf

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circuits that cannot fit onto a single FPGA **chip**, the field programmable interconnect **chip** (FPIC) Empirical results show that the method is **time**-efficient and applicable to large layout problem of the FPGA is connected to an FPIC pin through a **trace** on the board. An FPIC does not implement any
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Modeling of DRAM Power Control Policies - Using Deterministic And (Correct)
complex policies and our results show that DRAM **chip** should always immediately transition to standby with decreasing power consumption but increasing **time** to transition back to Active. We must design a distribution, and validated our model against **trace**-driven simulations. Our results show that, for
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to put more resources on a single microprocessor **chip** than ever before. However, by putting more

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1 Real-time interval logic for reasoning about executions of real-time programs
R. Razouk, M. Gorlick
November 1989 **ACM SIGSOFT Software Engineering Notes , Proceedings of the ACM SIGSOFT '89 third symposium on Software testing, analysis, and verification**, Volume 14 Issue 8
Full text available: pdf(935.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Research on the testing and debugging of distributed real-time programs now focuses on more formal approaches to specification and testing. Temporal logic is a natural candidate for this since it can specify properties of event and state sequences. However, the absence of any concept of real-time limits the application of temporal logic to non real-time behavior. This paper presents an extension of the interval logic of Schwartz et al. [SMSVP83], by increasing the expressive power of the lo ...

2 A real-time microprocessor debugging technique
Charles R. Hill
March 1983 **Proceedings of the symposium on High-level debugging**, Volume 18 , 8 Issue 8 , 4
Full text available: pdf(380.29 KB) Additional Information: full citation, abstract, references

This note describes RED, a remotely executed debugger capable of generating a real-time source level trace history of a high level language program executing on a microprocessor. The trace history consists of a display of the source statements of each basic block executed, annotated by the time at which execution of that block began. Basic blocks are traced rather than statements to reduce sampling bandwidth requirements while still retaining the ability to record the essential logical flow of p ...

3 Saving traces for Ada debugging
Carol H. LeDoux, D. Stott Parker
May 1985 **ACM SIGAda Ada Letters , Proceedings of the 1985 annual ACM SIGAda international conference on Ada**, Volume V Issue 2
Full text available: pdf(732.37 KB) Additional Information: full citation, abstract, references, citings, index terms

A trace database model for debugging concurrent Ada programs is presented. In this approach, trace information is captured in an historical database and queried using Prolog. This model was used to build a prototype debugger, called Your Own Debugger for Ada (YODA). The design of YODA is described and a trace analysis of a sample program exhibiting misuse of shared data is presented. Because the trace database model is flexible and general, it can aid diagnosis of a variety of runtime errors.

4 Ada debugging and testing support environments

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1 Poster Session 1: On-chip delay measurement for silicon debug

Ramyanshu Datta, Antony Sebastine, Ashwin Raghunathan, Jacob A. Abraham

April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available: pdf(113.39 KB) Additional Information: full citation, abstract, references, index terms

Efficient test and debug techniques are indispensable for performance characterization of large complex integrated circuits in deep-submicron and nanometer technologies. Performance characterization of such chips requires on-chip hardware and efficient debug schemes in order to reduce time to market and ensure shipping of chips with lower defect levels. In this paper we present an on-chip scheme for delay fault detection and performance characterization. The proposed technique allows for accurat ...

Keywords: delay fault testing, design for testability, silicon debug

2 Debug Support, Calibration and Emulation for Multiple Processor and Powertrain Control SoCs

A. Mayer, H. Siebert, K. D. McDonald-Maier

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 3**

Full text available: pdf(222.95 KB) Additional Information: full citation, abstract

The introduction of complex SoCs with multiple processor cores presents new development challenges, such that development support is now a decisive factor when choosing a System-on-Chip (SoC). The presented developments support strategy addresses the challenges using both architecture and technology approaches. The Multi-Core Debug Support (MCDS) architecture provides flexible triggering using cross triggers and a multiple core break and suspend switch. Temporal trace ordering is guaranteed down ...

3 Session 8D: embedded tutorial: Test of future system-on-chips

Yervant Zorian, Sujit Dey, Michael J. Rodgers

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(140.88 KB) Additional Information: full citation, abstract, references, citings

Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. Being able to rapidly develop, manufacture, test, debug and verify complex SOCs is crucial for the continued success of the electronics industry. This growth is expected to continue full force at least for the next decade, while making possible the production of multimillion transistor chips. However, to mak ...

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